REMARKS

The Applicants request reconsideration of the rejection.

Claims 1-12 are pending.

Claims 1, 2, 4-8, and 11 were rejected under 35 U.S.C. § 102(b) as being anticipated by Hanaoka et al U.S. Patent No. 5,521,590 (Hanaoka).

In order to support a rejection for anticipation under §102(b), the applied reference must teach, expressly or inherently, each limitation set forth in the rejected claims. In the present case, the Applicants submit that claims 1-2, 4-8, and 11 are patentably distinguishable from Hanaoka based, at least, on Hanaoka's lack of any teaching or suggestion to provide the claimed RFID with a semiconductor circuit device whose impedance is maintained at a low impedance state when the device is in the reset (inactive) state.

In this regard, the Applicants thank the Examiner for the careful explanation of applying the teachings of Hanaoka against the claims. Of particular note is the explanation that the Examiner considers the data output OUTDATA of the data carrier main circuit 100 to be "understood" as low (or logic 0) when the data carrier main circuit 100 is in the off or reset state, causing transistor T1 to close and to maintain the data carrier 200 in a low impedance state.

Respectfully, after a careful analysis of the patent disclosure and Figure 8 in particular, the Applicants submit that the Examiner errs in determining that OUTDATA is necessarily at logic 0 when the data carrier main circuit 100 is inactive.

Referring to Figure 8, transistor T4 (switch 15) takes the ON state when a voltage V_{S1} exceeds a fixed voltage V_{ON}, such that electric power is supplied on the power source line V_{S2}. Immediately after the electric power is supplied on the power source line V_{S2}, the logic circuit of the data carrier main circuit 100 is controlled into an initial state by power-on reset circuit 14, and enters the standby state. Then, communication by modulation of alternating-current magnetic field can begin. The transistor T4 takes the OFF state when the voltage V_{S1} is less than a minimum operation voltage V_{OFF}. Therefore, supply of electric power on the power source line V_{S2} is interrupted when transistor T4 turns OFF, whereby the data carrier main circuit 100 does not operate (enters the inactive state).

As shown in Figure 8, the data carrier main circuit 100 is always connected to the reference potential line V_{DD}, even when switch 15 is open. On the other hand, when switch 15 (transistor T4) is open, there is no power supplied to line

V_{S2}, so that the voltage of the output data OUTDATA is either (a) the voltage of the reference potential line V_{DD}, or (b) floating. The voltage of the output data OUTDATA in case (b) depends on the voltage immediately before the switch 15 is opened. Thus, it is not true that the voltage of the output data OUTDATA is always low when the data carrier main circuit 100 is in the reset, or inactive, state. Therefore, transistor T1 is not necessarily in the ON state when the data carrier main circuit 100 is inactive (that is, when switch 15 is open or transistor T4 is OFF).

In fact, it is more likely that the voltage of the output data OUTDATA, when the data carrier main circuit 100 is in the floating state, approaches the voltage V_{DD}, because a switching element having an infinitely large resistance would be required to control the modulator circuit 2 in the OFF state. Of course, a switching element having infinitely large resistance does not exist.

In summary, when switch 15 (transistor T4) of Hanaoka is open,

(a) in the case where the voltage of the output data OUTDATA is the voltage of the reference potential line V_{DD}, the transistor T1 is in the OFF state and the impedance state seen from the coil 1 is maintained in the high state, or

b) in the case where the voltage of the output data OUTDATA is in the floating state, the ON/OFF state of transistor T1 becomes indefinite and the high/low impedance state seen from the coil 1 becomes indefinite. Therefore, Hanaoka cannot be said to maintain the impedance of the semiconductor device in the low impendence state when in the reset, or inactive, state.

Each of the independent claims is limited by requiring that the impedance of the semiconductor device be maintained at the low impedance state when the device is in the reset state. Therefore, each of the independent claims, and by extension each of the dependent claims, patentably defines over Hanaoka.

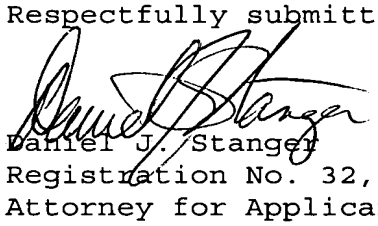
Claim 3 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Hanaoka as applied to claim 1 above, and further in view of Hirano et al U.S. Patent No. 6,246,624 (Hirano). Claims 9, 10, and 12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hanaoka in view of Beigel U.S. Patent No. 5,973,598 (Beigel). Because neither Hirano nor Beigel discloses or is cited as disclosing the feature of maintaining a semiconductor device at the low impedance state when the device is in the reset state, the combination of Hanaoka with either Hirano or Beigel cannot legally render

obvious the invention claimed in claims 3, 9, 10, and 12. Therefore, each of these claims patentably defines over the prior art.

The Applicants request an interview with the Examiner at a mutually convenient time to be determined in the near future, after the Applicants' representative has submitted an agenda for the interview deemed acceptable by the Examiner and her supervisor. The Applicants' representative requests a telephone call if the agenda has not been received at the time the Examiner is required to act on this Reply.

In view of the foregoing remarks, the Applicants request reconsideration of the rejection and allowance of the claims.

Respectfully submitted,



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